

Figure 1

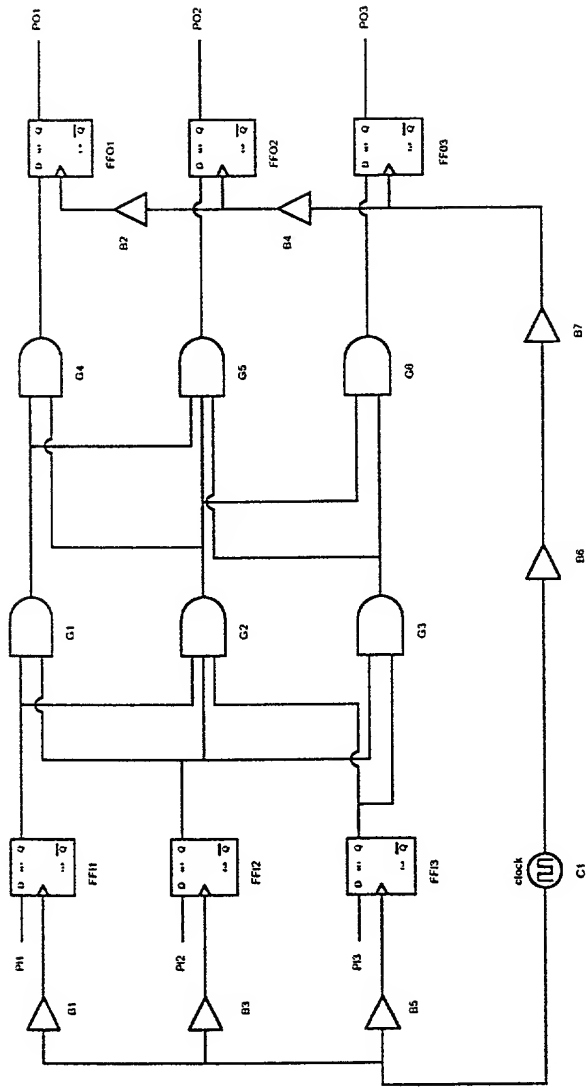
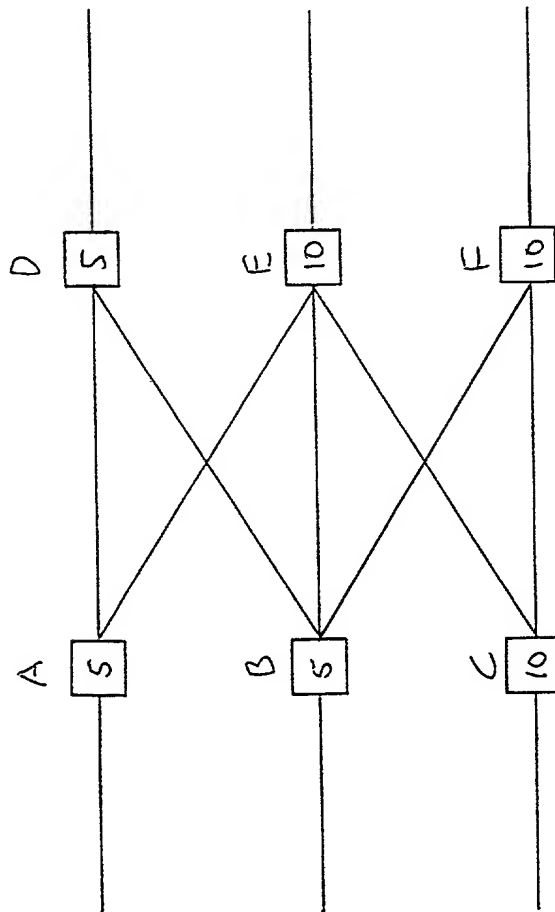


FIGURE 2A



1200T

1000T

Figure 2B

# Forward Delay Sums

$$\begin{array}{r} A \\ \hline (5) \\ \hline \end{array}$$

$$\begin{array}{r} B \\ \hline (5) \\ \hline \end{array}$$

$$\begin{array}{r} C \\ \hline (10) \\ \hline \end{array}$$

$$\begin{array}{r} D \\ \hline (10) \\ \hline 10 \end{array}$$

$$\begin{array}{r} E \\ \hline (15) \\ \hline 15 \\ \hline 20 \end{array}$$

$$\begin{array}{r} F \\ \hline (15) \\ \hline 20 \\ \hline \end{array}$$

Figure 3

$T_{\phi}$	$T_s$	$T_{ij}$	HOLD TIME CONSTRAINT	MINIMUM FORWARD DELAY SUM	MAXIMUM FORWARD DELAY SUM	SETUP TIME CONSTRAINT	OUTPUT NODE
2	12	9	7	10	10	26	D
2	3	8	6	15	20	35	E
2	19	10	8	15	20	19	F

Clock Period = 40

Setup Time Constraint = Clock Period -  $T_{\phi}$  -  $T_s$

Hold Time Constraint =  $T_{ij}$  -  $T_{\phi}$

FIGURE 4

# Reverse Delay Differences

$$\begin{array}{r} D \\ \hline 21 \end{array}$$

$$\begin{array}{r} E \\ \hline 25 \end{array}$$

$$\begin{array}{r} F \\ \hline 9 \end{array}$$

$$\begin{array}{r} A \\ \hline 16 \\ 20 \end{array}$$

$$\begin{array}{r} B \\ \hline 16 \\ 20 \\ \hline 4 \end{array}$$

$$\begin{array}{r} C \\ \hline 15 \\ -1 \end{array}$$

Figure 5

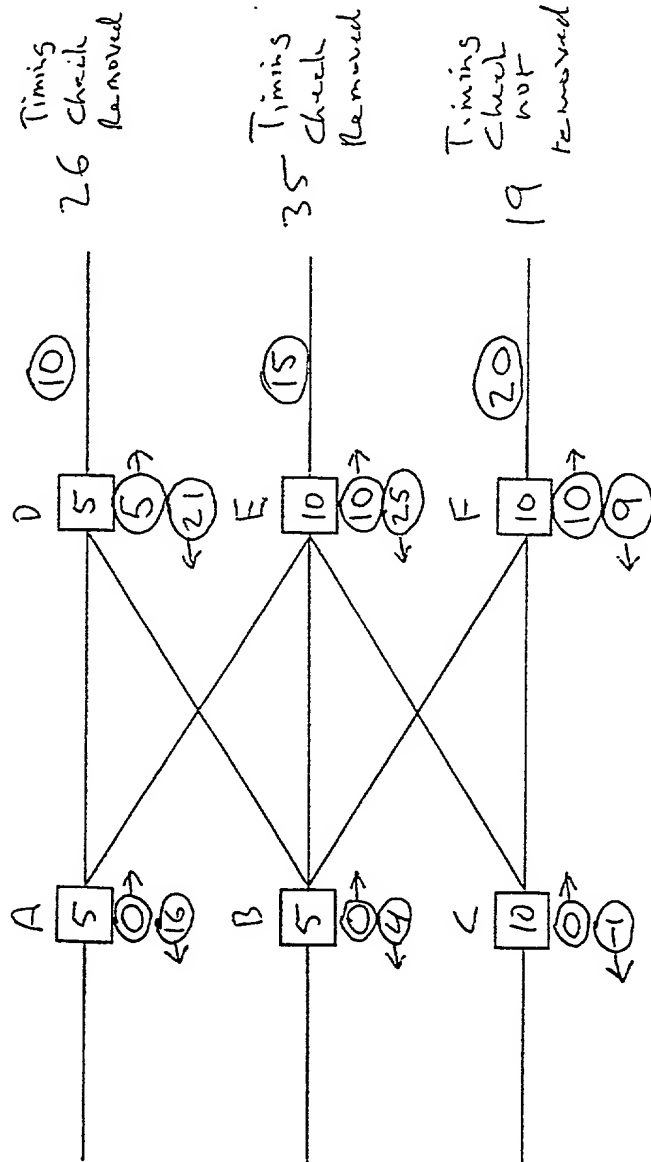


Figure 6

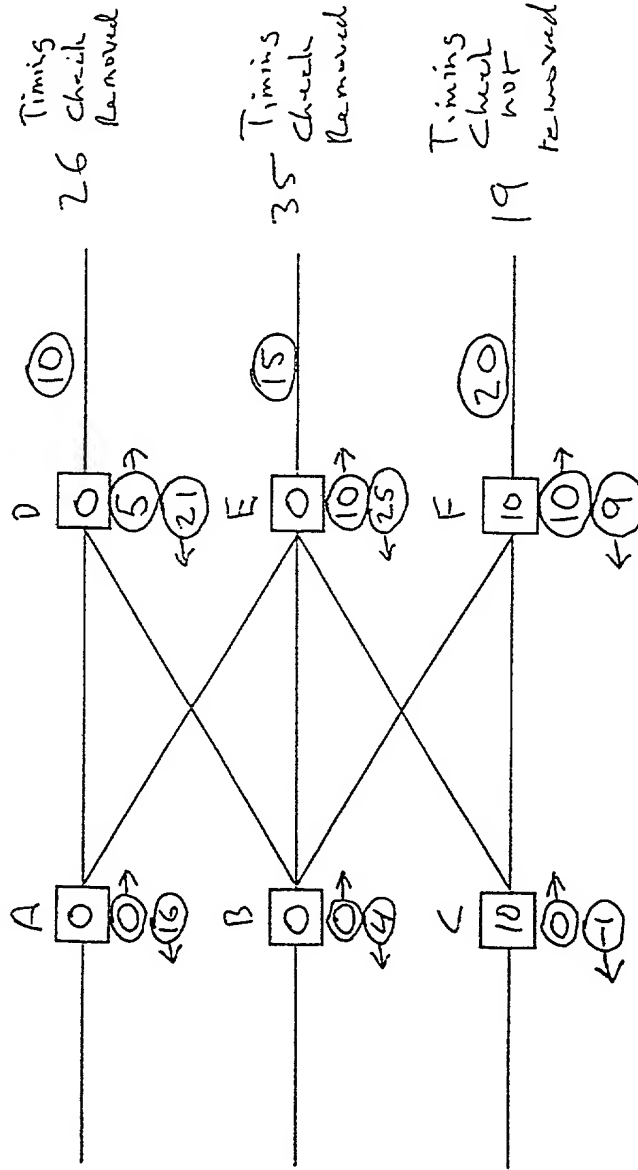


Figure 7A



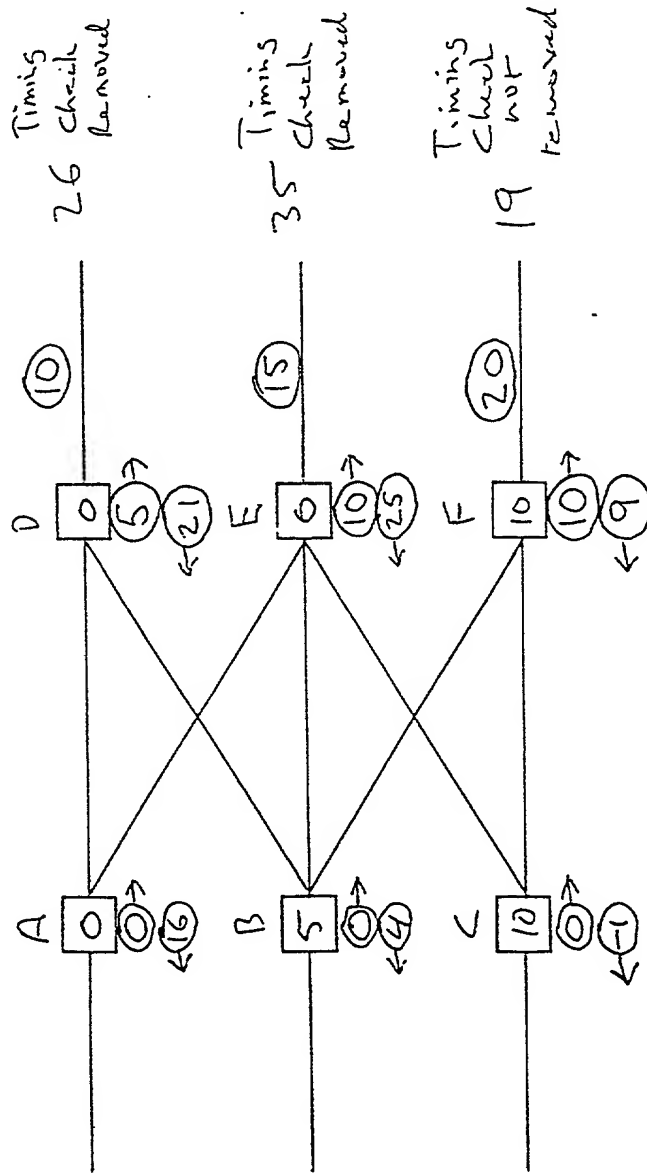


Figure 7 B

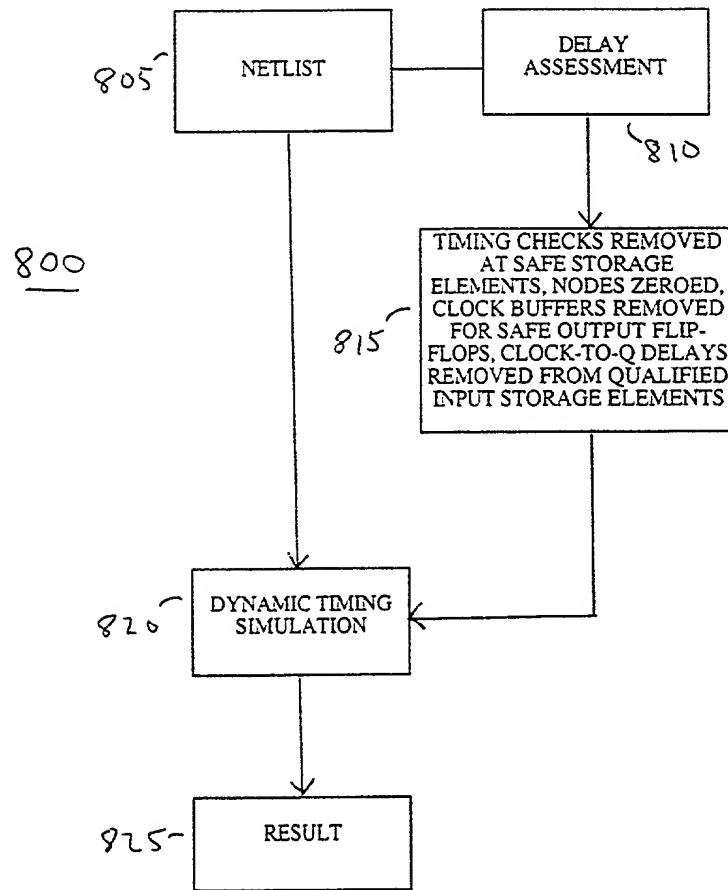


FIGURE 8

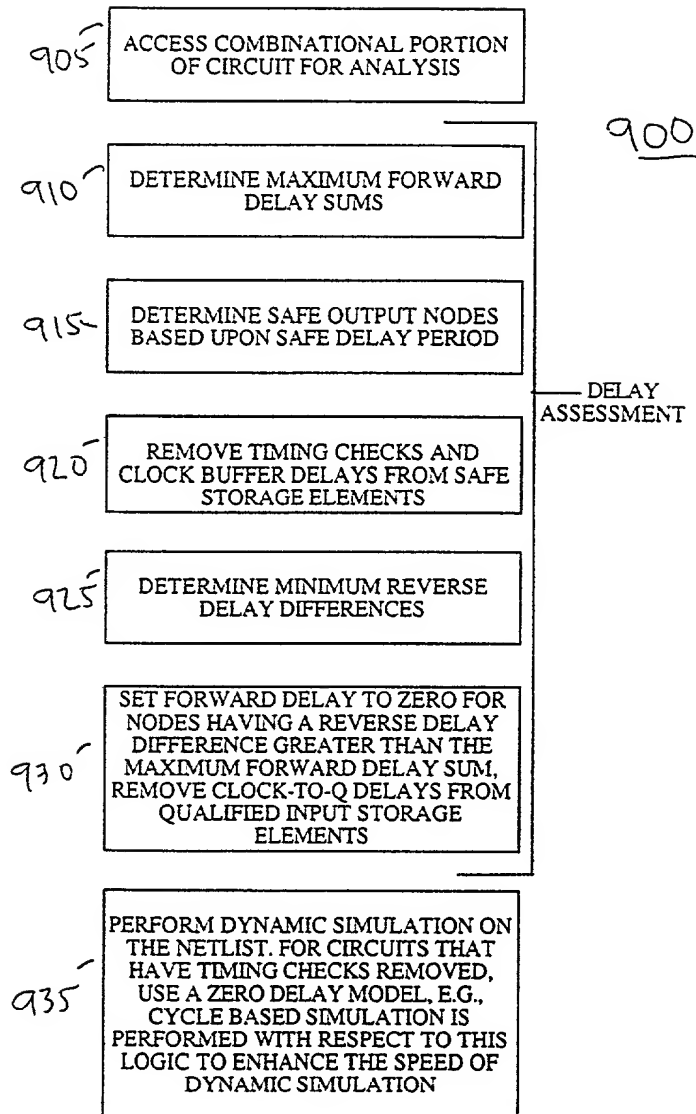


FIGURE 9